WEST Search History

DATE: Tuesday, January 04, 2005

Hide?	Set Name	Query	Hit Count
		DB=JPAB; PLUR=YES; OP=ADJ	
☐	L25	L24 and (host or computer or CPU or processor or microprocessor or station)	12
☐	L24	L23 and synchroniz$ adj4 clock$	46
☐	L23	(memory or RAM or DRAM) and (alternat$ or switch$) adj5 clock$	567
☐	L22	L20 and synchroniz$ adj4 clock$	99
☐	L21	L20 and synchroniz$	220
☐	L20	(memory or RAM or DRAM) and (select$ or alternat$ or switch$) adj5 clock$	1148
		DB=PGPB,USPT; PLUR=YES; OP=ADJ	
☐	L19	L8 and (host or CPU or computer or processor)	51
☐	L18	L17 and clock$ adj6 gat$	0
☐	L17	L16 and (host or CPU or computer or processor)	83
☐	L16	L15 and (dual$ or single$)	97
☐	L15	L7 and (select$ or alternat$ or switch$) adj5 clock$ adj5 (first or second)	116
☐	L14	L13 and clock$ adj6 gat$	0
☐	L13	L12 and gate	319
☐	L12	L11 and synchroniz$ adj3 clock$	381
☐	L11	L10 and asynchronous$	429
☐	L10	l7 and (host or CPU or computer or processor)	943
☐	L9	L8 and (dual$ or single$)	51
☐	L8	L7 and (alternat$ or switch$) adj5 clock$ adj5 (first or second)	62
☐	L7	L6 and synchroniz$ adj4 clock$	1143
☐	L6	L5 and clock signal	2595
☐	L5	L4 and read$ and writ$	3673
☐	L4	L3 and (alternat$ or switch$) adj3 clock$	4933
☐	L3	L2 and clock	82473
☐	L2	L1 and (DRAM or RAM)	238006
☐	L1	memory	687844

END OF SEARCH HISTORY

WEST Search History

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Hide?	Set Name	Query	Hit Count
		DB=USPT; PLUR=YES; OP=ADJ	
☐	L27	L26 and (select$ or alternat$ or switch$) adj5 clock$	49
☐	L26	17 and (single-port or dual-port)	49
		DB=JPAB; PLUR=YES; OP=ADJ	
☐	L25	L24 and (host or computer or CPU or processor or microprocessor or station)	12
☐	L24	L23 and synchroniz$ adj4 clock$	46
☐	L23	(memory or RAM or DRAM) and (alternat$ or switch$) adj5 clock$	567
☐	L22	L20 and synchroniz$ adj4 clock$	99
☐	L21	L20 and synchroniz$	220
☐	L20	(memory or RAM or DRAM) and (select$ or alternat$ or switch$) adj5 clock$	1148
		DB=PGPB,USPT; PLUR=YES; OP=ADJ	
☐	L19	L8 and (host or CPU or computer or processor)	51
☐	L18	L17 and clock$ adj6 gat$	0
☐	L17	L16 and (host or CPU or computer or processor)	83
☐	L16	L15 and (dual$ or single$)	97
☐	L15	L7 and (select$ or alternat$ or switch$) adj5 clock$ adj5 (first or second)	116
☐	L14	L13 and clock$ adj6 gat$	0
☐	L13	L12 and gate	319
☐	L12	L11 and synchroniz$ adj3 clock$	381
☐	L11	L10 and asynchronous$	429
☐	L10	17 and (host or CPU or computer or processor)	943
☐	L9	L8 and (dual$ or single$)	51
☐	L8	L7 and (alternat$ or switch$) adj5 clock$ adj5 (first or second)	62
☐	L7	L6 and synchroniz$ adj4 clock$	1143
☐	L6	L5 and clock signal	2595
☐	L5	L4 and read$ and writ$	3673
☐	L4	L3 and (alternat$ or switch$) adj3 clock$	4933
☐	L3	L2 and clock	82473
☐	L2	L1 and (DRAM or RAM)	238006
☐	L1	memory	687844